CMOS SILICIDE METAL GATE INTEGRATION

ABSTRACT OF THE DISCLOSURE

The present invention provides a complementary metal oxide semiconductor integration process whereby a plurality of silicided metal gates are fabricated atop a gate dielectric. Each silicided metal gate that is formed using the integration scheme of the present invention has the same silicide metal phase and substantially the same height, regardless of the dimension of the silicide metal gate. The present invention also provides various methods of forming a CMOS structure having silicided contacts in which the polySi gate heights are substantially the same across the entire surface of a semiconductor structure.